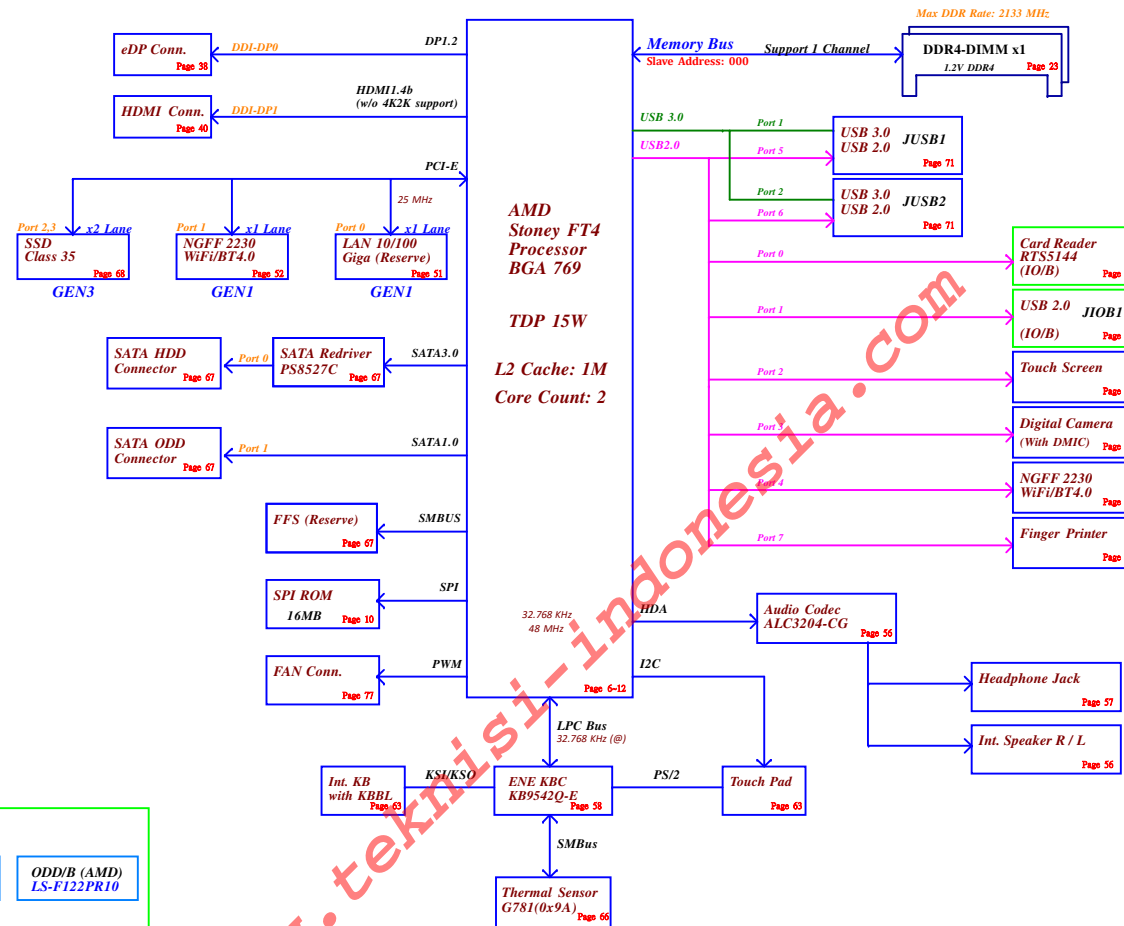


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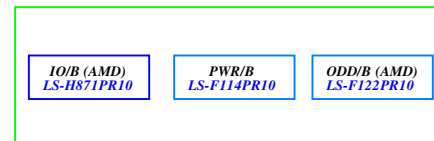
Dell / Compal Confidential
Schematic Document
AMD Stoney Ridge

2018-05-21 Rev: 1.0 (A00)

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SUB-BOARDS



Board ID Table for AD Channel:

Vcc	3.3V +/- 1%
Ra[RE5]	100K +/- 1%

Board ID	Rh(RE9)	VAD_min	VAD_typ	VAD_max	EC AD3
0	0 ohm	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.919V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table:

Board ID	Definition
0	N3V3 MLK STR UMA <EVT>
1	N3V3 MLK STR UMA <DVT1>
2	N3V3 MLK STR UMA <DVT2>
3	N3V3 MLK STR UMA <PVT>
4	N/A
5	N/A
6	N/A
7	N/A
8	N/A
9	N/A
10	N/A
11	N/A
12	N/A
13	N/A
14	N/A
15	N/A
16	N/A
17	N/A
18	N/A
19	N/A

Symbol Note :

 : Means Digital Ground

 : Means Analog Ground

SMBUS Control Table:

	SOURCE	BATT	Charger	Thermal Sensor	Touch Pad	DIMM	FFS
EC_SMB_CR1 EC_SMB_DA1	KB9542Q	V	V				
EC_SMB_CR2 EC_SMB_DA2	KB9542Q			V			
TP_CLK TP_DATA	KB9542Q				V		
APU_SCLK0 APU_SDATA0	APU					V	V
APU_SIC APU_SID	APU			V			

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+5VALW	System +5VALW power rail	ON	ON	ON*
+3VALW	System +3VALW power rail	ON	ON	ON*
+1.8V_ALW	System +1.8VALW power rail	ON	ON	ON*
+0.95VALW	System +0.95VALW power rail	ON	ON	ON*
+0.775VALW	System +0.775VALW power rail	ON	ON	ON*
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF
+0.6V_DDR_VTT	DDR4 +0.6V power rail	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+0.95VS	System +0.95VS power rail	ON	OFF	OFF
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Core NB voltage for APU	ON	OFF	OFF
+VDDCR_FCH_ALW	S5 supply voltage for the FCH core logic	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON
+0.95VS_APU_GFX	PCIe GPP, PCIe GFX, DP and SATA PHY logic power rail for APU	ON	OFF	OFF
+3VS_APU	+3VS power rail for APU	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

HS I/O

USB3.0

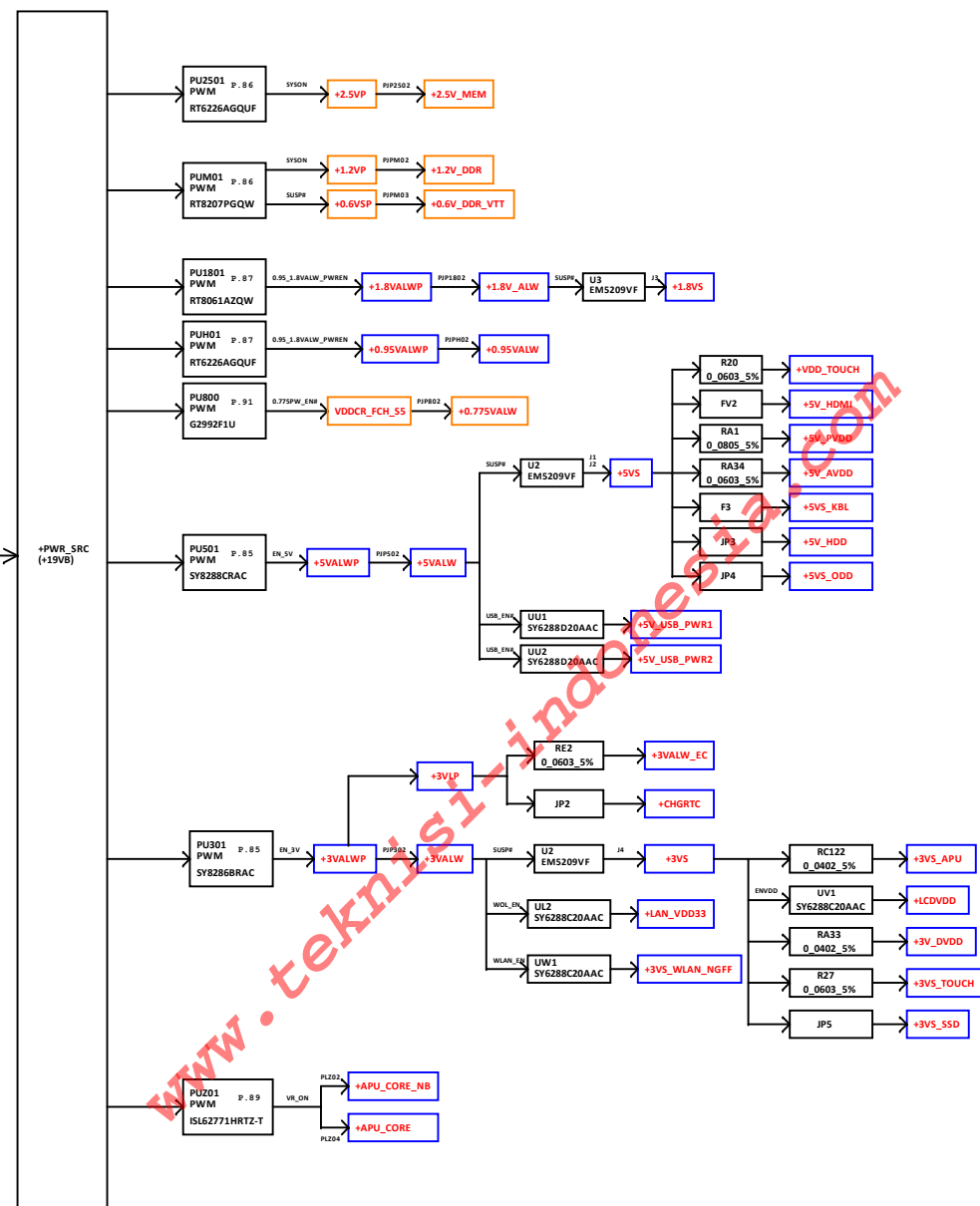
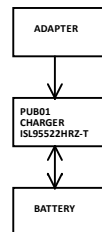
Port 0	---
Port 1	USB3 Connector Port 1
Port 2	USB3 Connector Port 2
USB2.0	
Port 0	Card Reader (IO/B)
Port 1	USB2 Connector Port (IO/B)
Port 2	Touch Screen
Port 3	Camera
Port 4	WLAN
Port 5	USB2 Connector Port 1
Port 6	USB2 Connector Port 2
Port 7	Finger Printer
SATA	
Port 0	HDD
Port 1	ODD
Display(DP)	
Port 0	eDP (Lan0/Lan1)
Port 1	HDMI (Lan0/Lan1/Lan2/Lan3)
Port 2	---

Clock Signal

GFX_CLK	---
GPP_CLK0	LAN
GPP_CLK1	WLAN
GPP_CLK2	NVMe SSD
GPP_CLK3	---
PCI Express(GFX)	
Lane 0	---
Lane 1	---
Lane 2	---
Lane 3	---
PCI Express(GPP)	
Lane 0	LAN
Lane 1	WLAN
Lane 2	NVMe SSD
Lane 3	NVMe SSD

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CPU PWR
Peripheral Device PWR

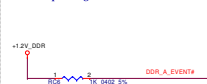


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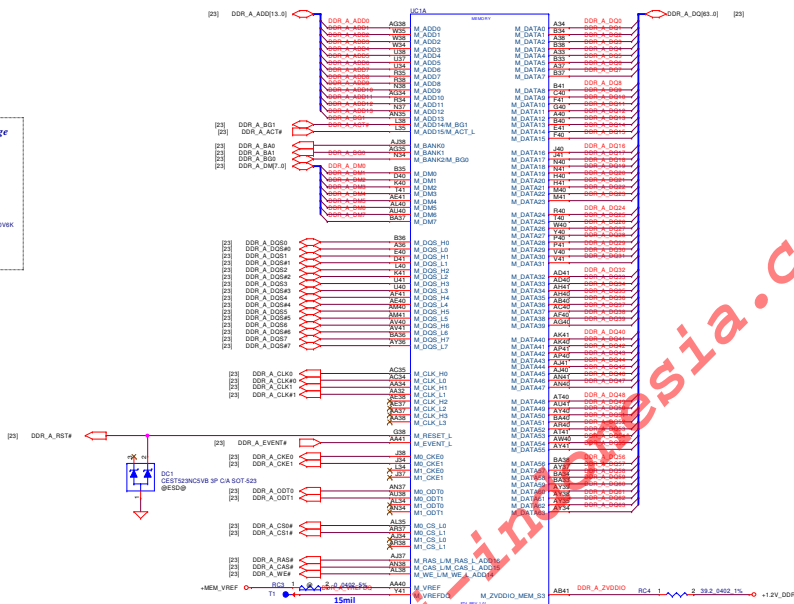
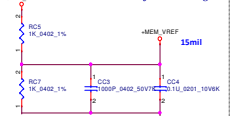
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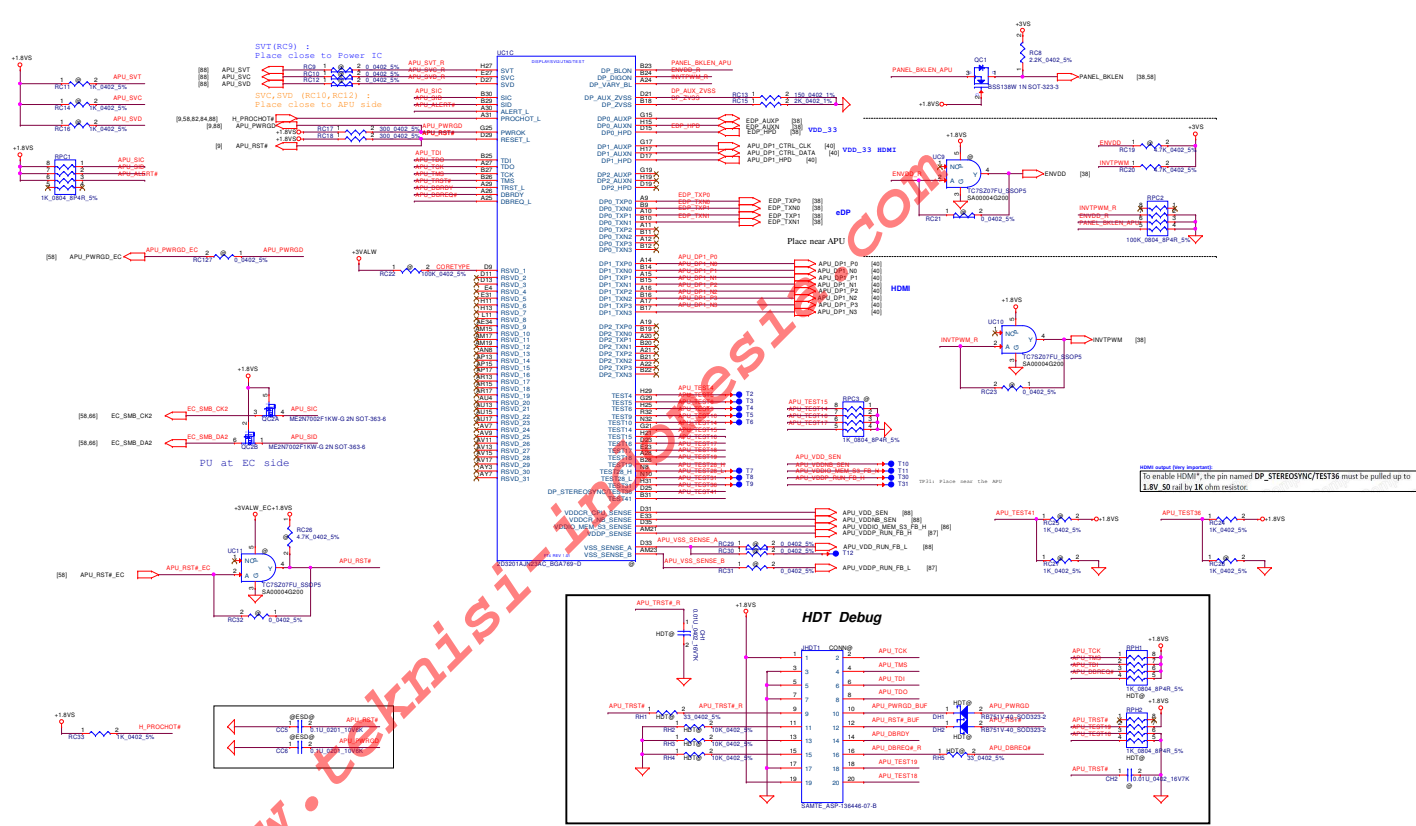
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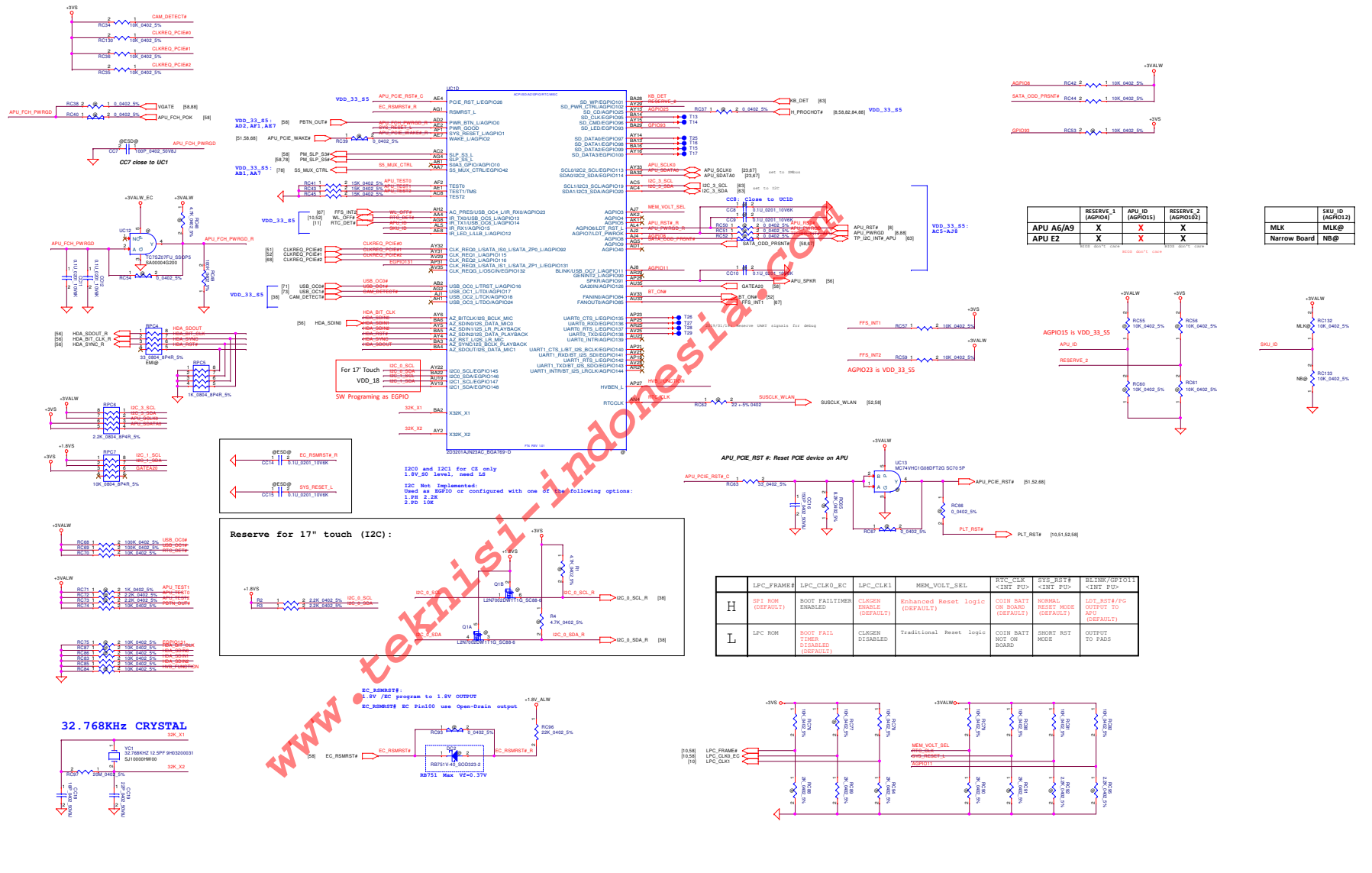


+1.2V_DDR



Place them close to APU within 1"





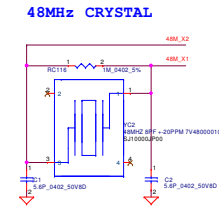
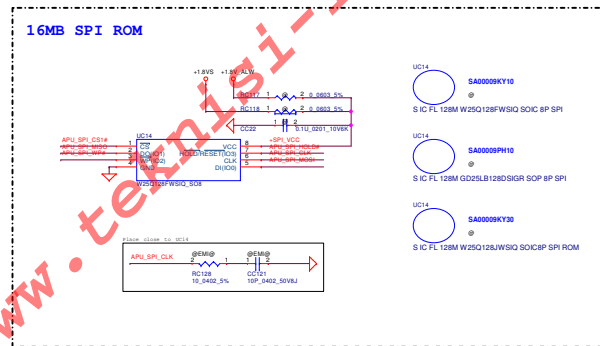
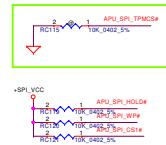
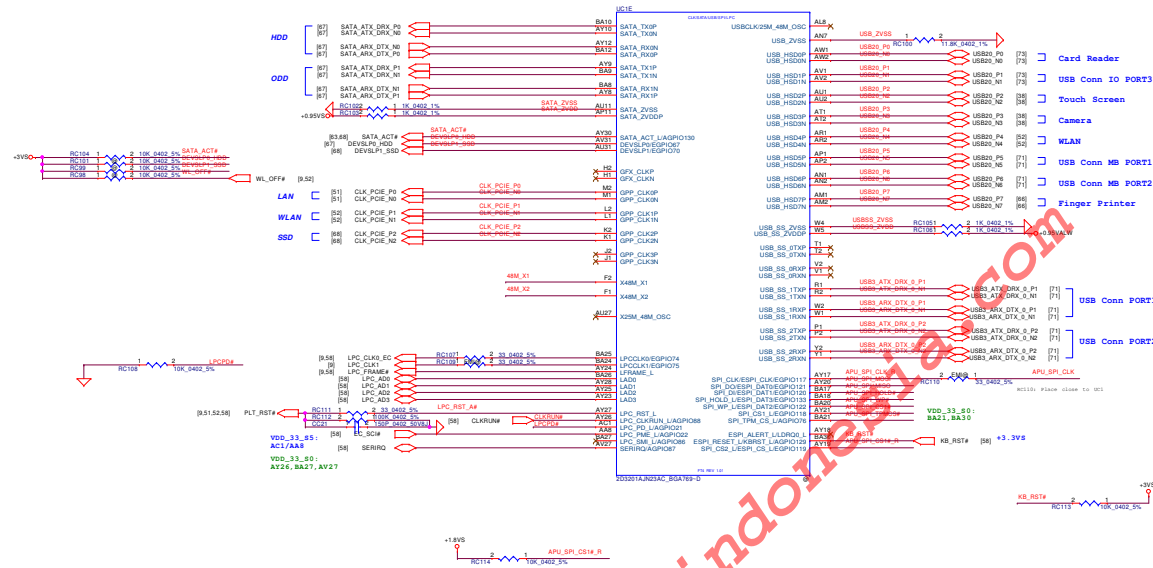
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APU A6/A9	X	X	X
APU E2	X	X	X

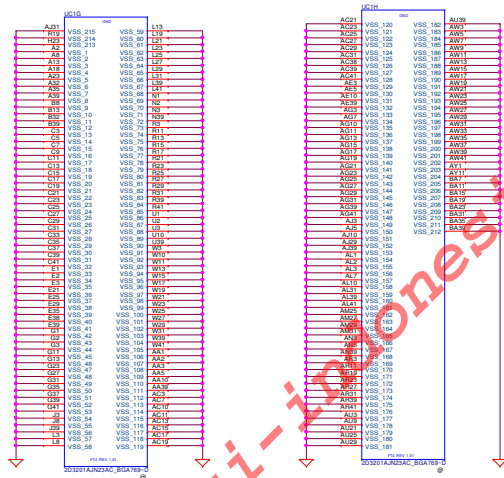
	SKU_ID (AP0P02)
MLK	MLK@
Narrow Board	NB@

	LPC_FRAME#	LPC_CLK0_EC	LPC_CLK1	MEM_VOLT_SEL	RTC_CLK <INT PU>	SYS_RST# <INT PU>	BLINK/OP011 <INT PU>
H	SPI ROM (DEFAULT)	BOOT FAILTIMER ENABLED	CLAKEN SHABLE (DEFAULT)	Enhanced Reset logic (DEFAULT)	COIN BATT ON BOARD (DEFAULT)	NORMAL RESET MODE (DEFAULT)	LDI_RST#/PG OUTPUT TO APU (DEFAULT)
L	LPC ROM	BOOT FAIL TIMER DISABLED (DEFAULT)	CLAKEN DISABLED	Traditional Reset logic	COIN BATT NOT ON BOARD	SHORT RST MODE	OUTPUT TO PAUD

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VDD_3.3_S5: Connect to +3VALW
VDD_3.3_S0: Connect to +3VS

[illegible]



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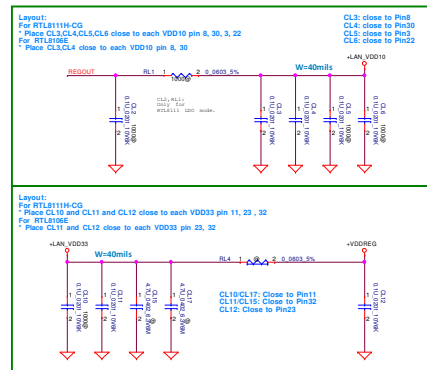
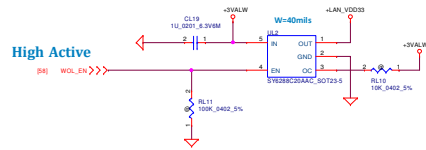
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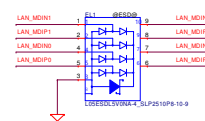
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The schematic shows the OPEN pin connected to +3VALW through a 20k resistor and to +LAN_VDD33 through another 20k resistor. The pin is also connected to JP6_@JUMP and JUMP_43X39.



	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111R-CG RTL8111G-CGT (71.08111.003)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

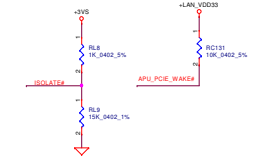
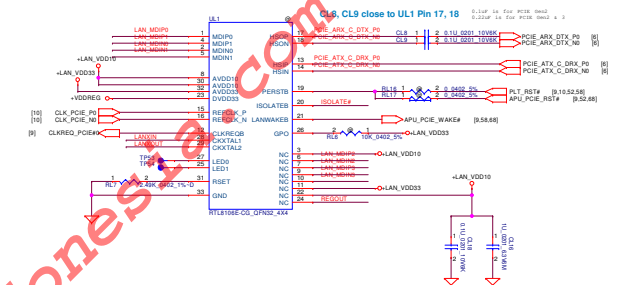
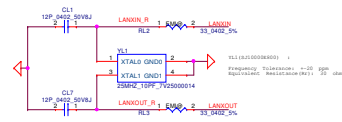


UL1 100Ω

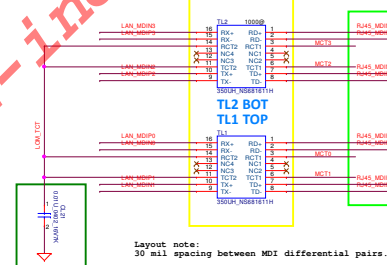
RTL8106E-CG_QFN32_4X4
SA000065Y00

UL1 1000g

RTL8111H-CG QFN32_4X4
SA000080P00

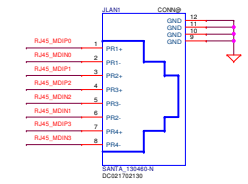
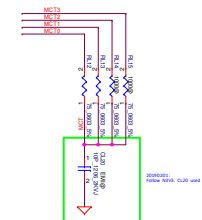


2019/02/11: For layout routing limitation, need to do P/W swap on TL



Main:
SP050009800, S X'FORM, NS681611H LAN

2nd:
SP050006W00, S X'FORM, HD-245 10/100 PC CARD LAN



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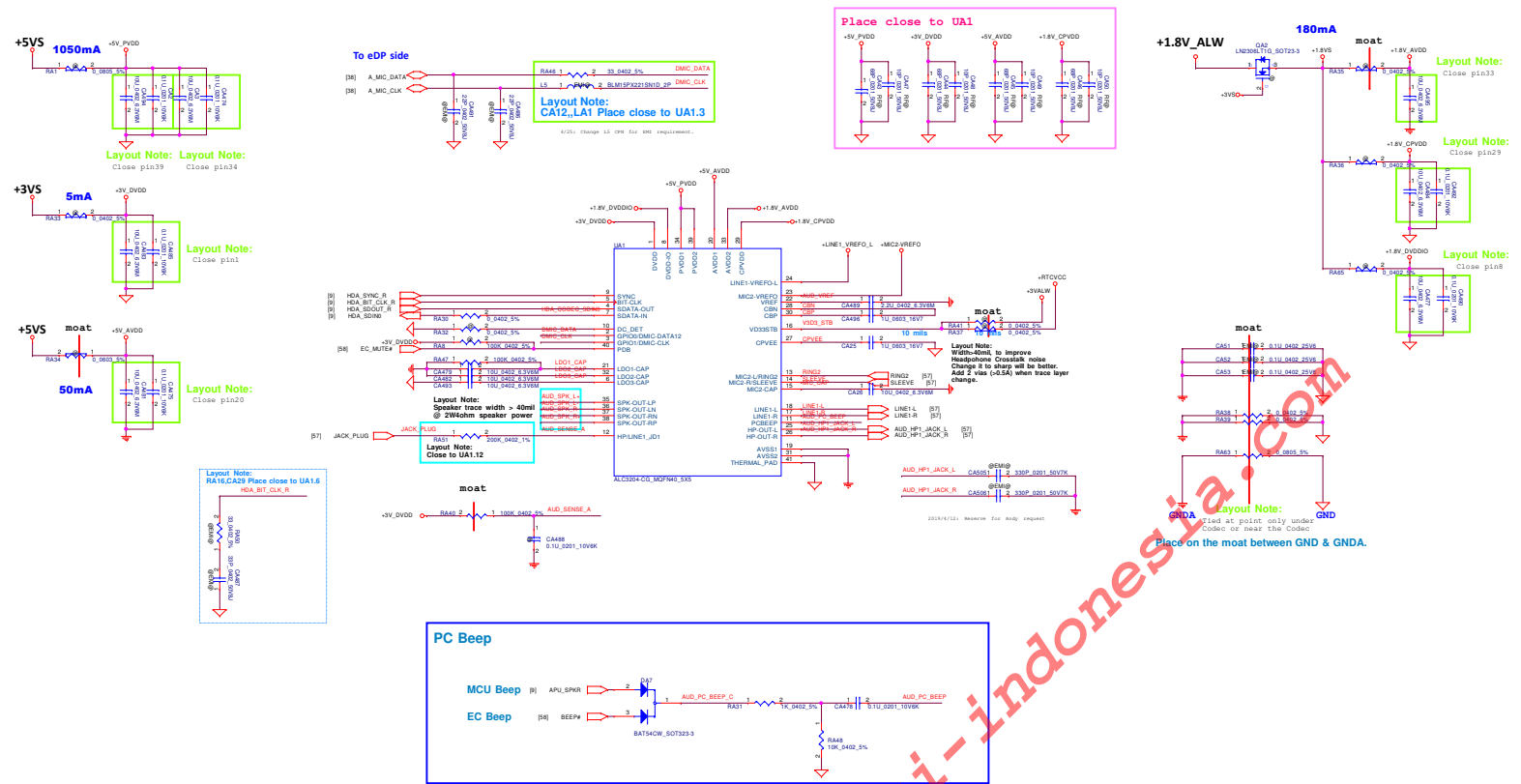
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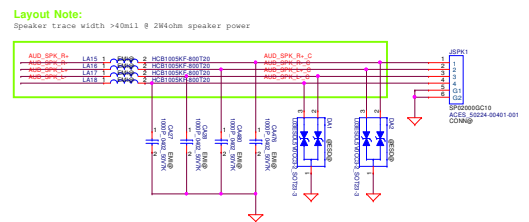
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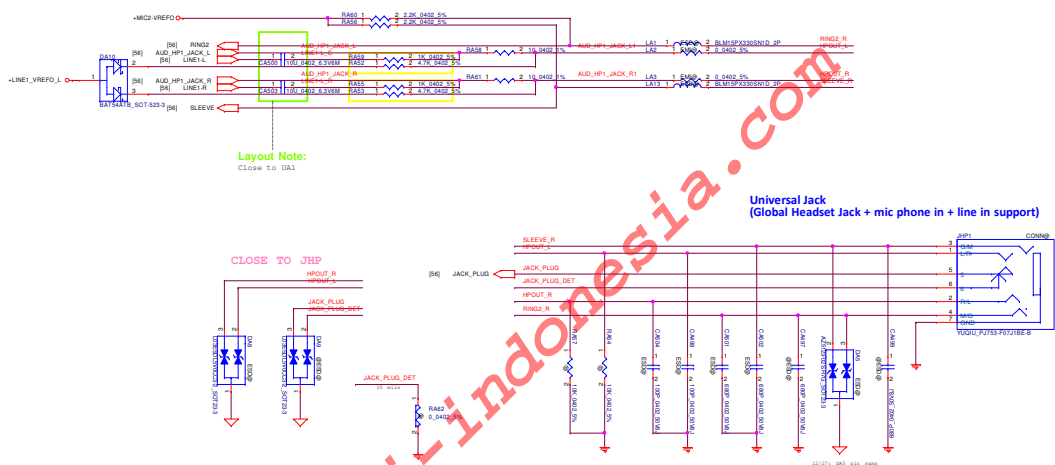
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Main Func = Audio

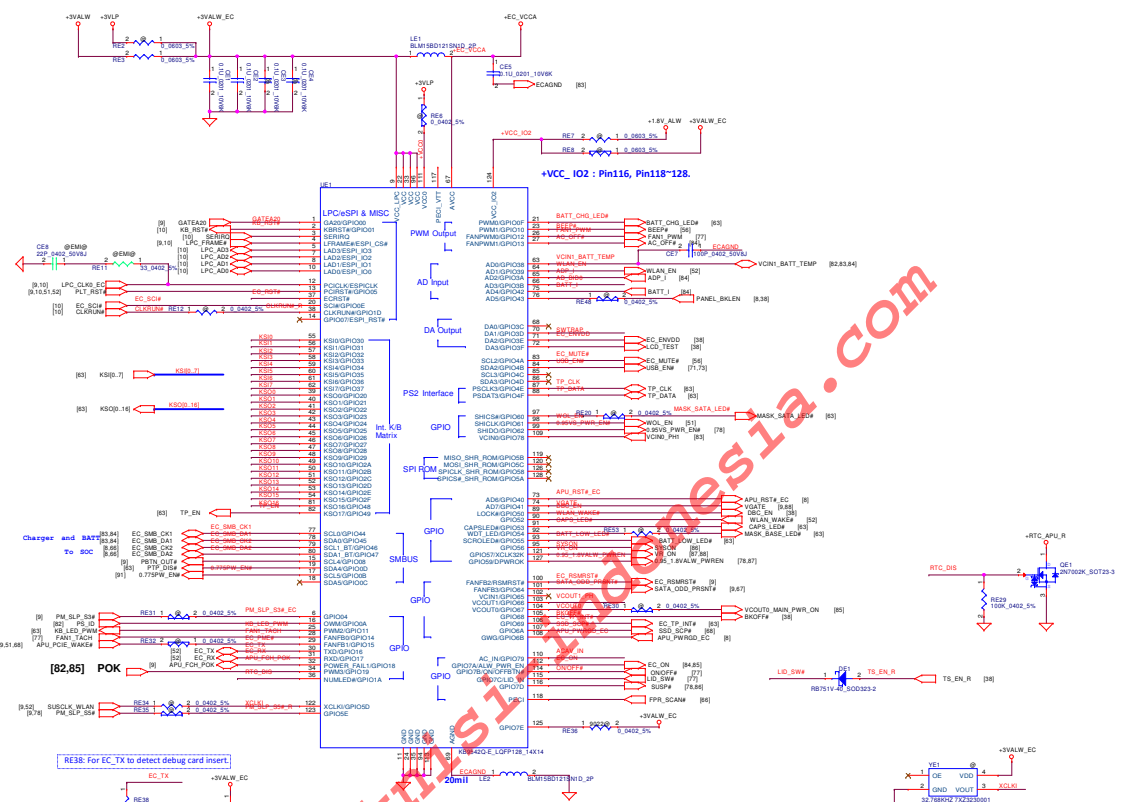
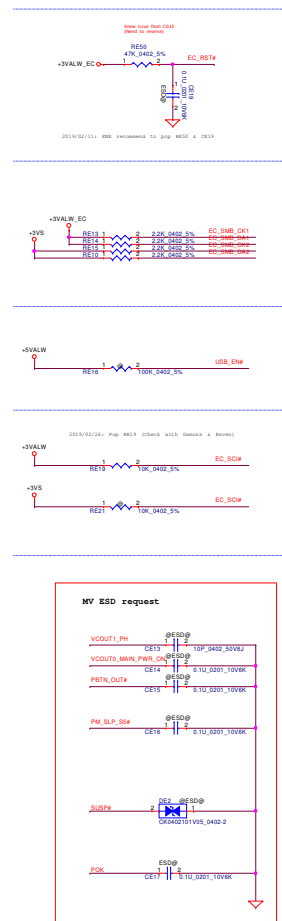


Main Func = Speaker



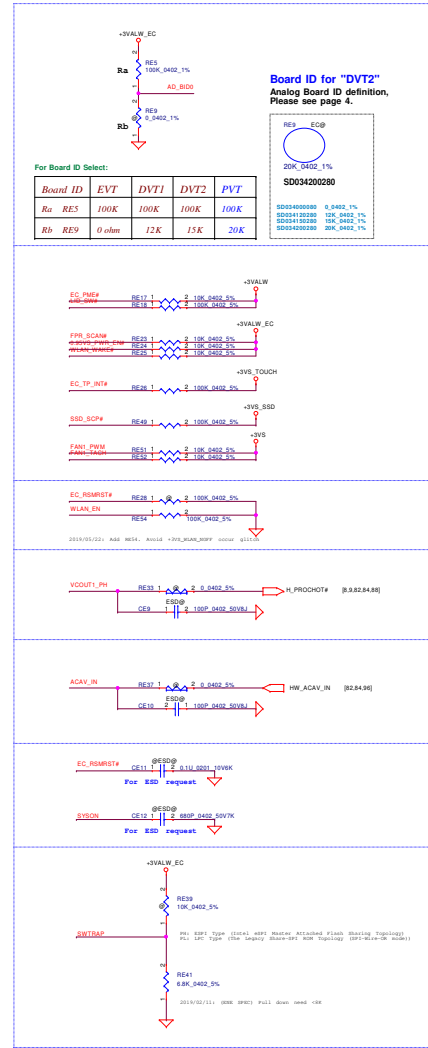


2019/03/21:
Change UE1 from B to E version.



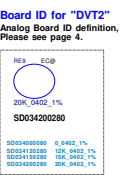
Charge and BATT

Component	Value	Notes
EC_SMB_CK1	100K	100K, 5%, 0.125W
EC_SMB_CK2	100K	100K, 5%, 0.125W
EC_SMB_CK3	100K	100K, 5%, 0.125W
EC_SMB_CK4	100K	100K, 5%, 0.125W
EC_SMB_CK5	100K	100K, 5%, 0.125W
EC_SMB_CK6	100K	100K, 5%, 0.125W
EC_SMB_CK7	100K	100K, 5%, 0.125W
EC_SMB_CK8	100K	100K, 5%, 0.125W
EC_SMB_CK9	100K	100K, 5%, 0.125W
EC_SMB_CK10	100K	100K, 5%, 0.125W
EC_SMB_CK11	100K	100K, 5%, 0.125W
EC_SMB_CK12	100K	100K, 5%, 0.125W
EC_SMB_CK13	100K	100K, 5%, 0.125W
EC_SMB_CK14	100K	100K, 5%, 0.125W
EC_SMB_CK15	100K	100K, 5%, 0.125W
EC_SMB_CK16	100K	100K, 5%, 0.125W
EC_SMB_CK17	100K	100K, 5%, 0.125W
EC_SMB_CK18	100K	100K, 5%, 0.125W
EC_SMB_CK19	100K	100K, 5%, 0.125W
EC_SMB_CK20	100K	100K, 5%, 0.125W
EC_SMB_CK21	100K	100K, 5%, 0.125W
EC_SMB_CK22	100K	100K, 5%, 0.125W
EC_SMB_CK23	100K	100K, 5%, 0.125W
EC_SMB_CK24	100K	100K, 5%, 0.125W
EC_SMB_CK25	100K	100K, 5%, 0.125W
EC_SMB_CK26	100K	100K, 5%, 0.125W
EC_SMB_CK27	100K	100K, 5%, 0.125W
EC_SMB_CK28	100K	100K, 5%, 0.125W
EC_SMB_CK29	100K	100K, 5%, 0.125W
EC_SMB_CK30	100K	100K, 5%, 0.125W
EC_SMB_CK31	100K	100K, 5%, 0.125W
EC_SMB_CK32	100K	100K, 5%, 0.125W
EC_SMB_CK33	100K	100K, 5%, 0.125W
EC_SMB_CK34	100K	100K, 5%, 0.125W
EC_SMB_CK35	100K	100K, 5%, 0.125W
EC_SMB_CK36	100K	100K, 5%, 0.125W
EC_SMB_CK37	100K	100K, 5%, 0.125W
EC_SMB_CK38	100K	100K, 5%, 0.125W
EC_SMB_CK39	100K	100K, 5%, 0.125W
EC_SMB_CK40	100K	100K, 5%, 0.125W
EC_SMB_CK41	100K	100K, 5%, 0.125W
EC_SMB_CK42	100K	100K, 5%, 0.125W
EC_SMB_CK43	100K	100K, 5%, 0.125W
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EC_SMB_CK98	100K	100K, 5%, 0.125W
EC_SMB_CK99	100K	100K, 5%, 0.125W
EC_SMB_CK100	100K	100K, 5%, 0.125W



Board ID Select:

Board ID	EVT	DVT1	DVT2	PVT
Ra	RES	100K	100K	100K
Rb	RES	0 ohm	12K	15K



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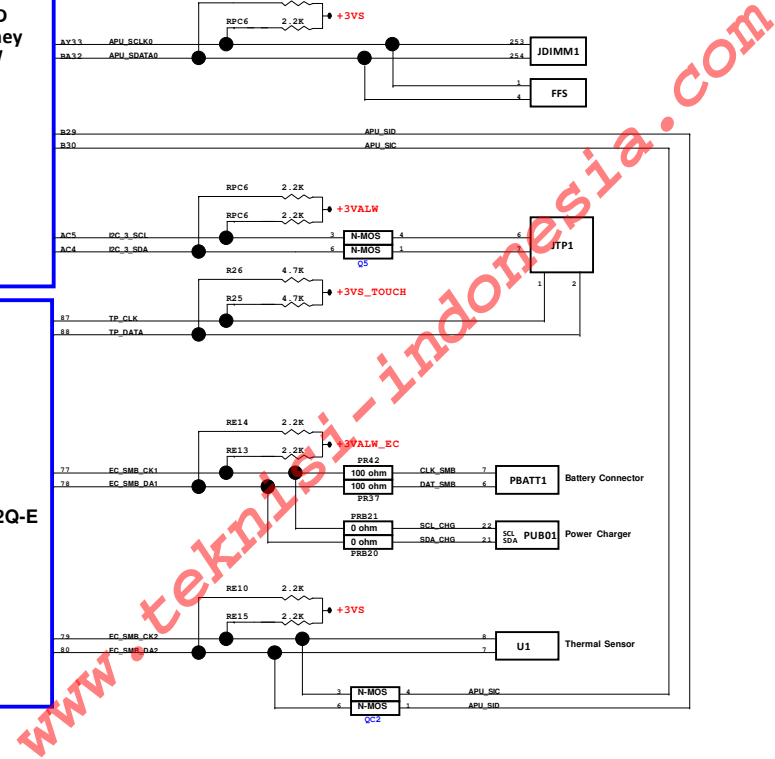
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Rev. D	LA-H872P		Rev. 1.0/001	Rev. 1.0/001

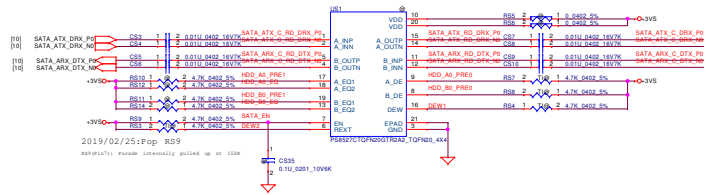
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Part	LA-H872P		Page	1 of 102

Main Func = HDD

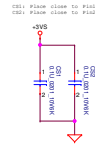
SATA X76 for BOM control:



2019/02/25: Update SATA re-driver strap table

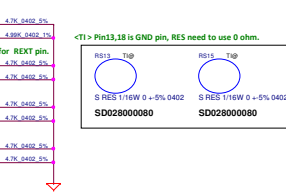
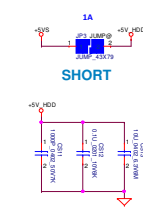
Pull High											
PIN	PIN 6	PIN 8	PIN 9	PIN 13	PIN 16	PIN 17	PIN 18	PIN 19		PIN 10	PIN 20
TI	DEW2	DE2	DE1	GND	DEW1	EQ1	GND	EQ2		VDD	VDD
PARADE	RXT	B_DE	A_DE	B_EQ2	DEW	A_EQ1	A_EQ2	B_EQ1		VDD	VDD
Location	RS3	RS8	RS7	RS14	RS4	RS10	RS12	RS11		RS5	RS6
TI	V	V	V	NC	V	NC	NC	NC		V	NC
Parade	NC	NC	NC	NC	NC	NC	NC	NC		V	V

Pull Down											
PIN	PIN 6	PIN 8	PIN 9	PIN 13	PIN 16	PIN 17	PIN 18	PIN 19		PIN 7	
TI	DEW2	DE2	DE1	GND	DEW	EQ1	GND	EQ2		EN	
PARADE	RXT	B_DE	A_DE	B_EQ2	DEW	A_EQ1	A_EQ2	B_EQ1		EN	
Location	RS16	RS18	RS20	RS15	RS17	RS19	RS13	RS21		RS9	
TI	NC	NC	NC	V	NC	V	V	V		V	
Parade	NC	NC	NC	NC	NC	NC	NC	NC		V	



2019/02/25: Change R519,R521 BOM structure to TI@

+5V_HDD Source



8.3.2 Output De-Emphasis

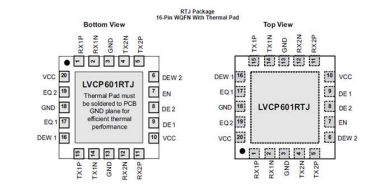
The SN75LVCP601 device provides the de-emphasis settings shown in Table 1. De-emphasis control is independent for each channel, controlled by the DE1 and DE2 pin settings as shown in Table 1. The reference for the de-emphasis settings available in the device is the transition bit amplitude for each given configuration; this transition bit amplitude is different at 0 dB than the -2-dB and -4-dB settings by design. DEW1 and DEW2 control the DE durations for channels one and two, respectively. Table 1 lists the recommended settings for these control pins. Output de-emphasis is capable of supporting FRM trace at the output anywhere from 2 in. (5.1 cm) to 12 in. (30.5 cm) at SATA 3G/6G speed.

Table 1. TX and RX EQ and DE Pulse-Duration Settings

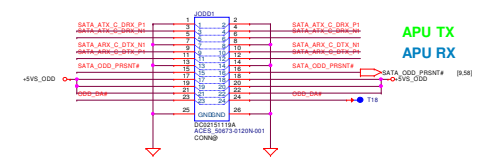
DE1 OR DE2		CH1 OR CH2 DE EMPHASIS (dB at 6 Gbps)		EQ1 OR EQ2		CH1 OR CH2 Equalization (dB at 6 Gbps)	
NC (default)	NC	-4	NC (default)	NC	0	7	PL RS19 / RS21
0	0	0	0	0	0	0	PH RS10 / RS11
1	1	-2	1	1	1	1	
DEW1 OR DEW2	DEW1 OR DEW2	DEVICE FUNCTION -- DE WIDTH FOR CH1/CH2					
0	0	De-emphasis pulse duration, short					
1 (default)	1 (default)	De-emphasis pulse duration, long					

SN75LVCP601
SATA 3G/6G 10-Pin WQFN With Thermal Pad
www.ti.com

5 Pin Configuration and Functions

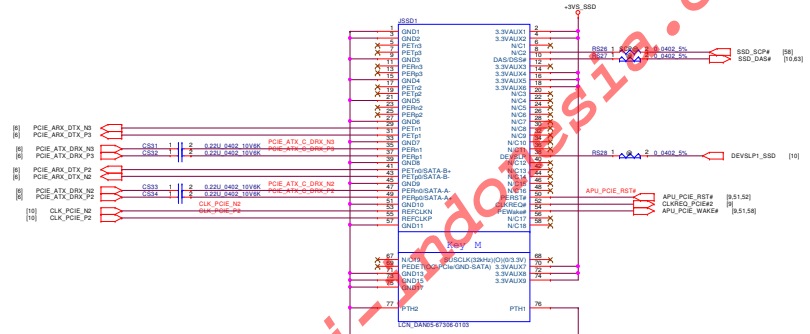
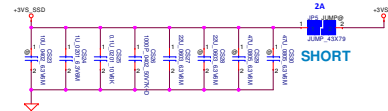


SATA ODD Connector (FFC Type)



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Doc. ID	LA-H872P	Doc. Name	LA-H872P	Rev. 1.0/001
Doc. No.	LA-H872P	Doc. Rev.	001	Rev. 1.0/001

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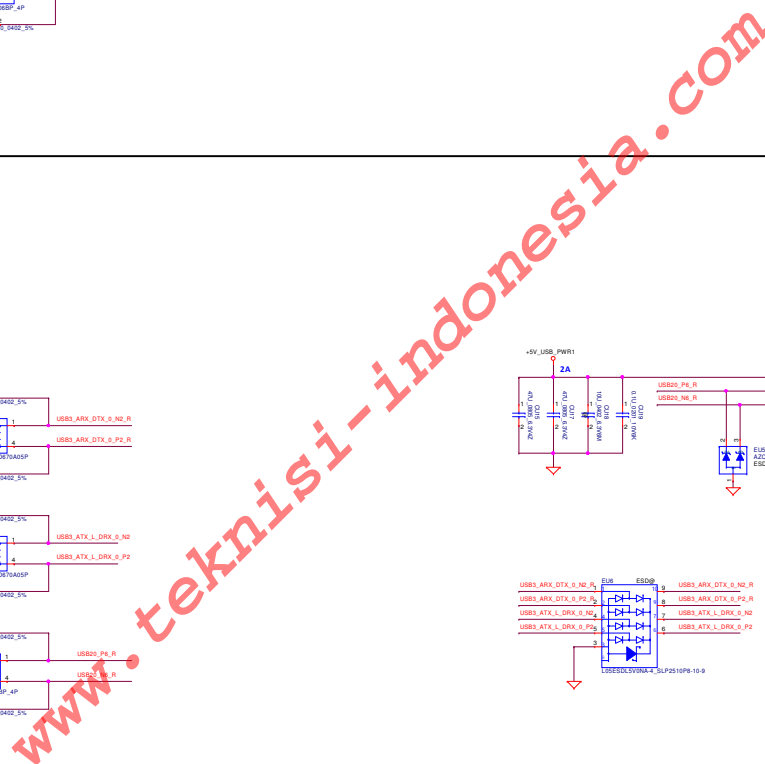
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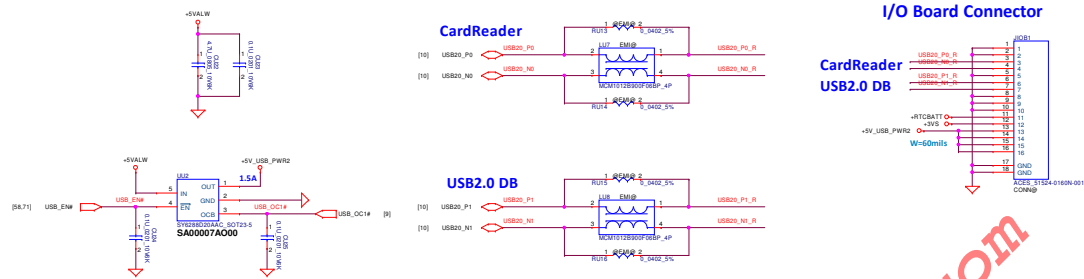
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Rev. D	LA-H872P		Rev. 1.0/001	Rev. 1.0/001

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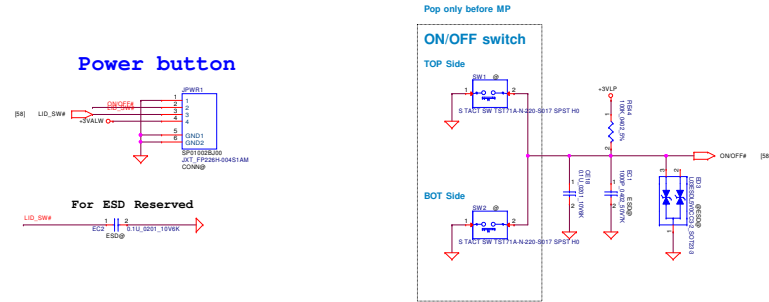
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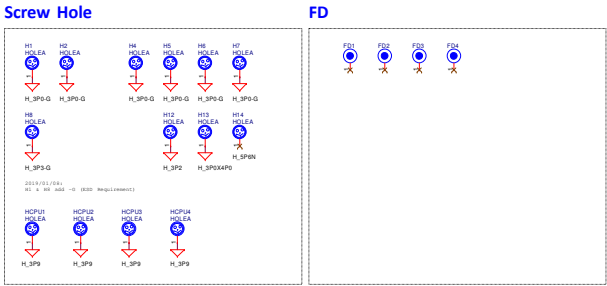
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Part	LA-H872P		Page	1 of 102

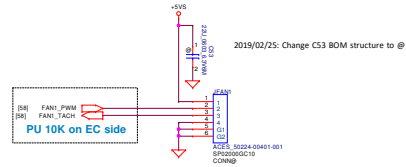
Main Func = POWER BTN



Main Func = Screw Hole



Main Func = FAN Control



Main Func = PCB P/N

Part Number	Description
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
PCB_R10@	

Part Number	Description
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
PCB_R10@	

Part Number	Description
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
PCB_R10@	

Part Number	Description
DA60026R000	PCB 20F LA-H872P REV0 M/B 3
PCB_R10@	

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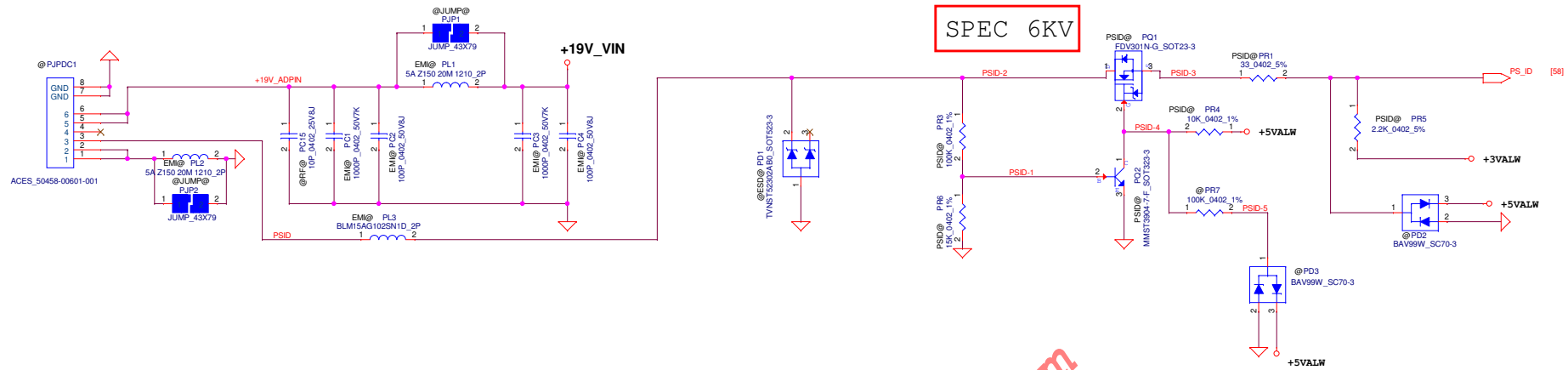
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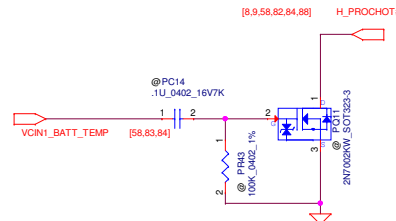
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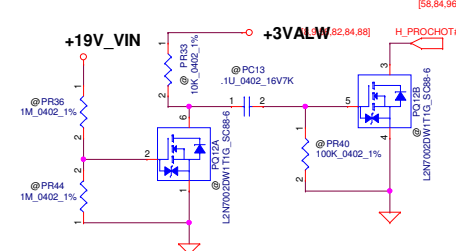
Adapter protection

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep it in BOM since battery can not be removed by end user

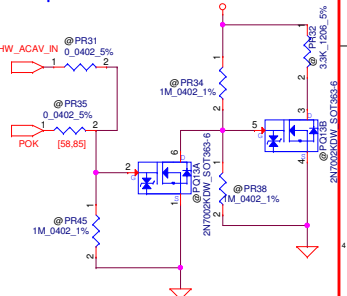


Battery protection

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW_PROCHOT# is issued by EC



Erp lot6 Circuit

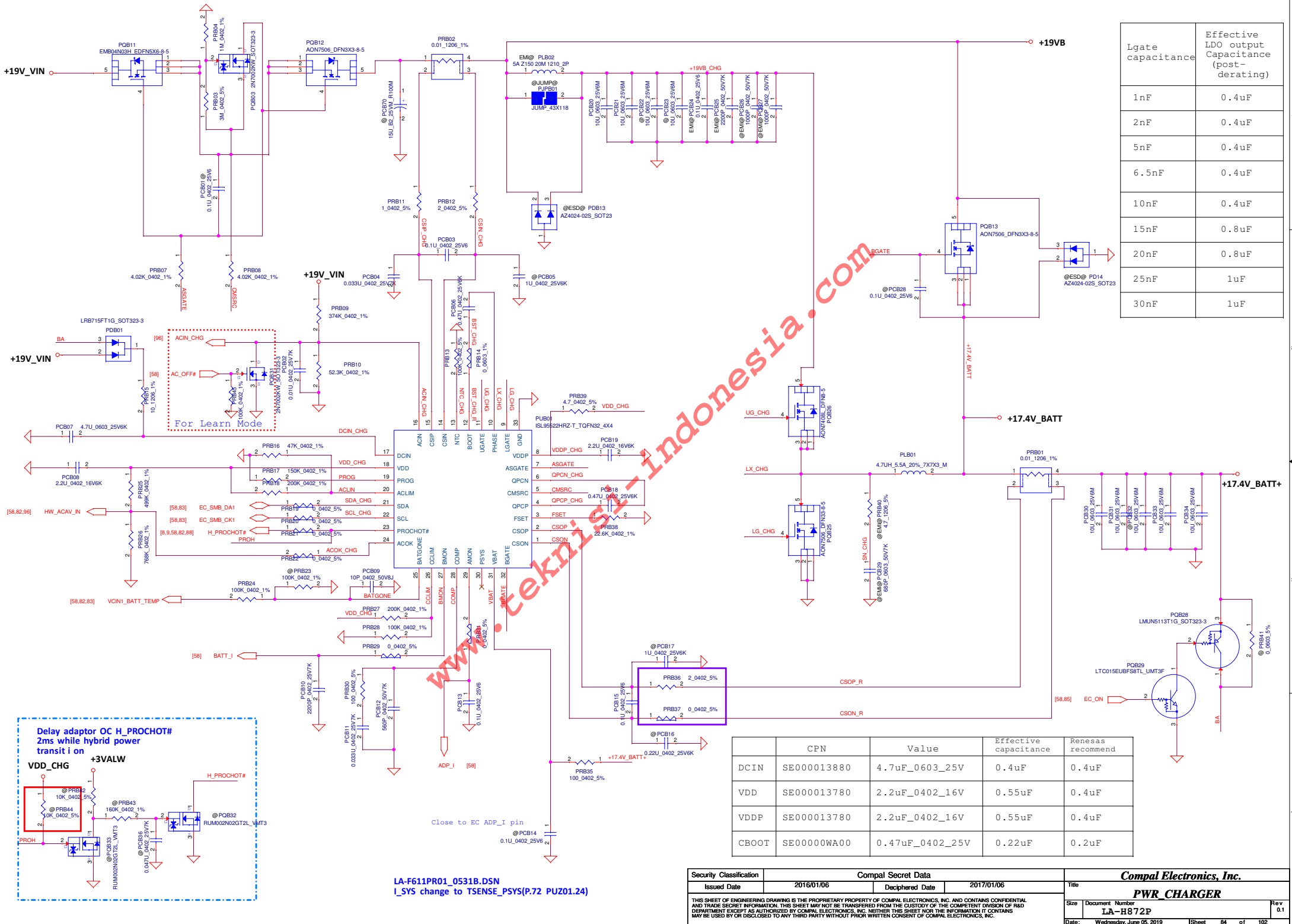


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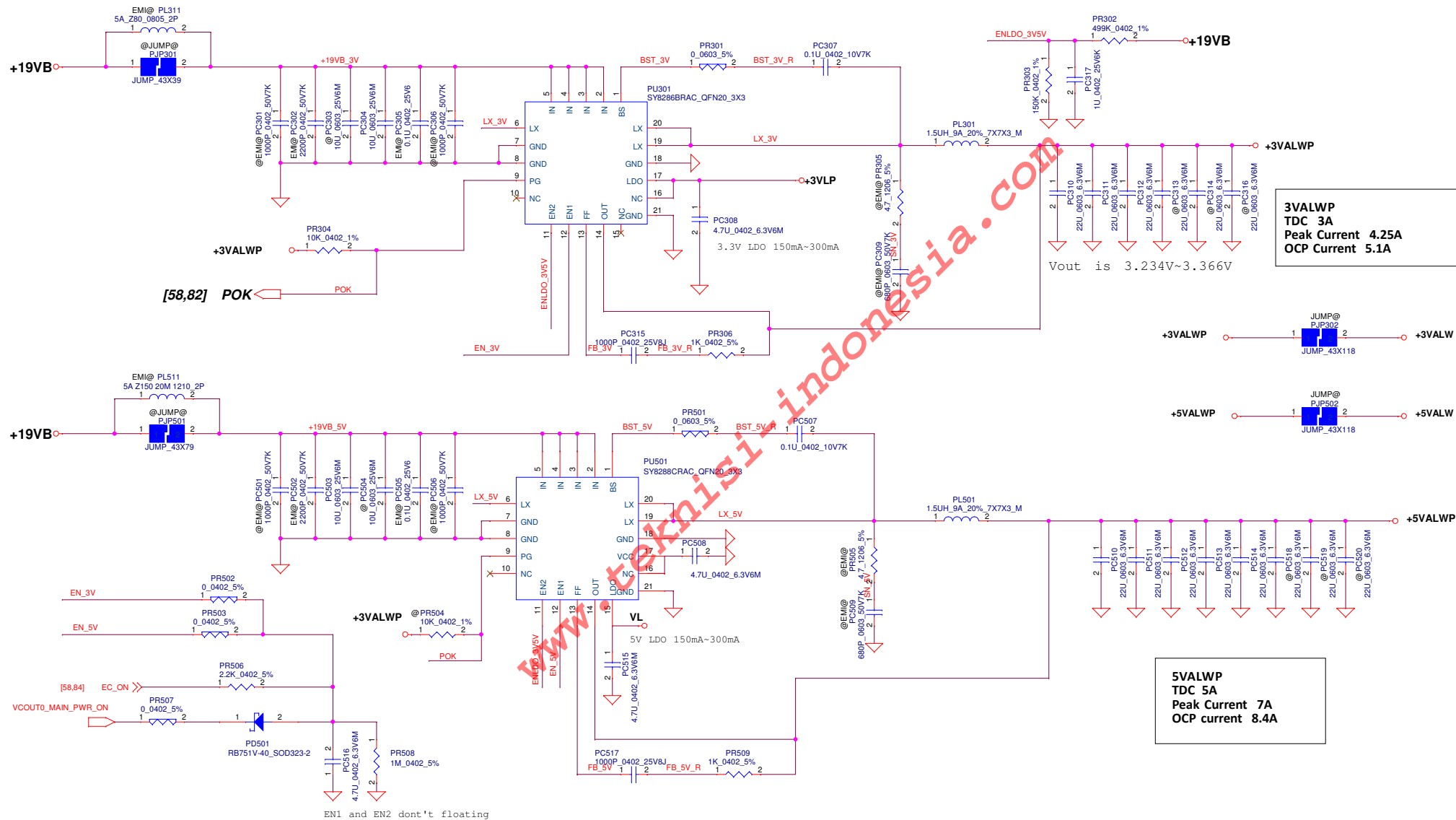
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Size	Document Number
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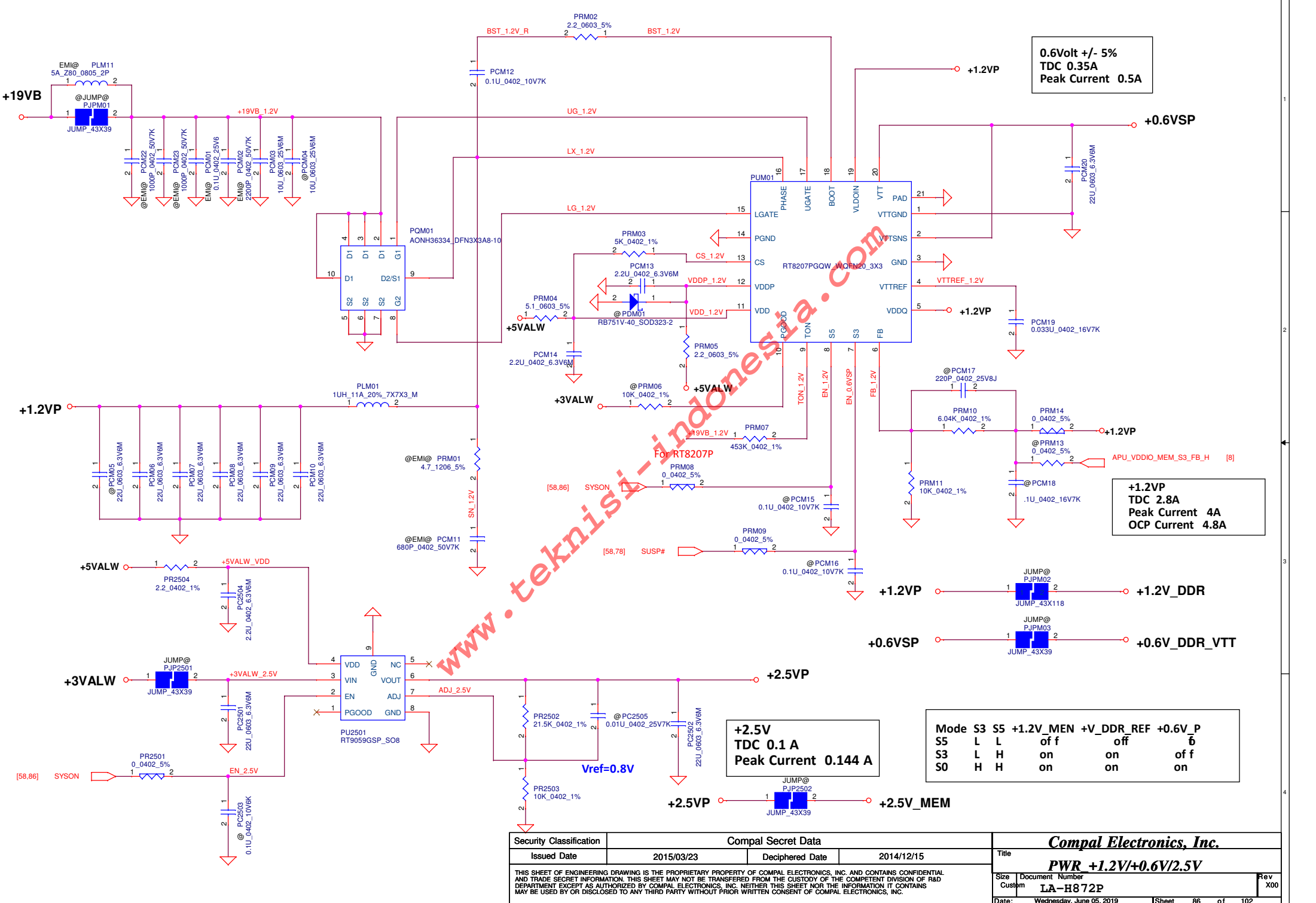
Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

	CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

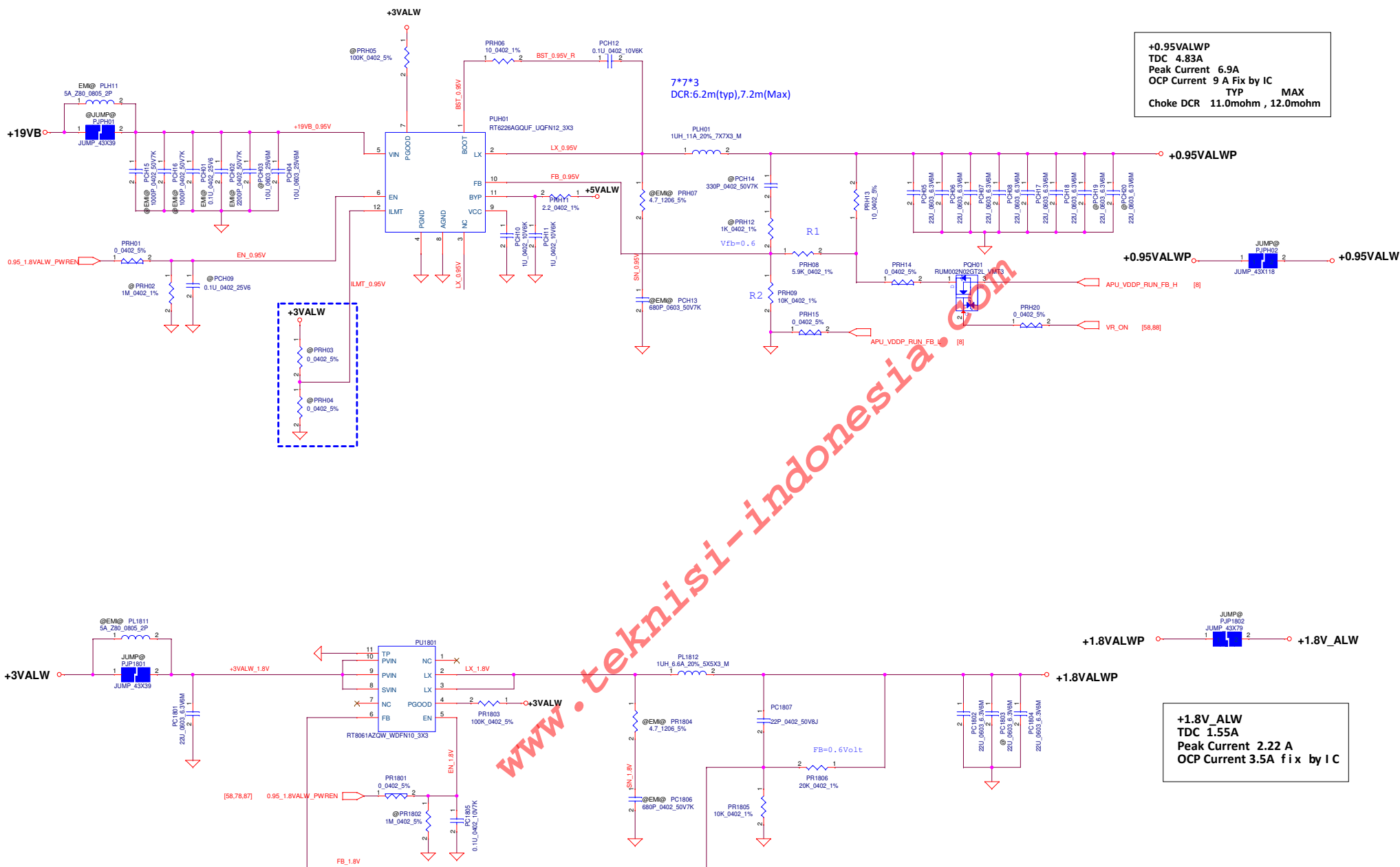
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I_SYS change to TSENSE_PSYS(P72 PUZ01.24)



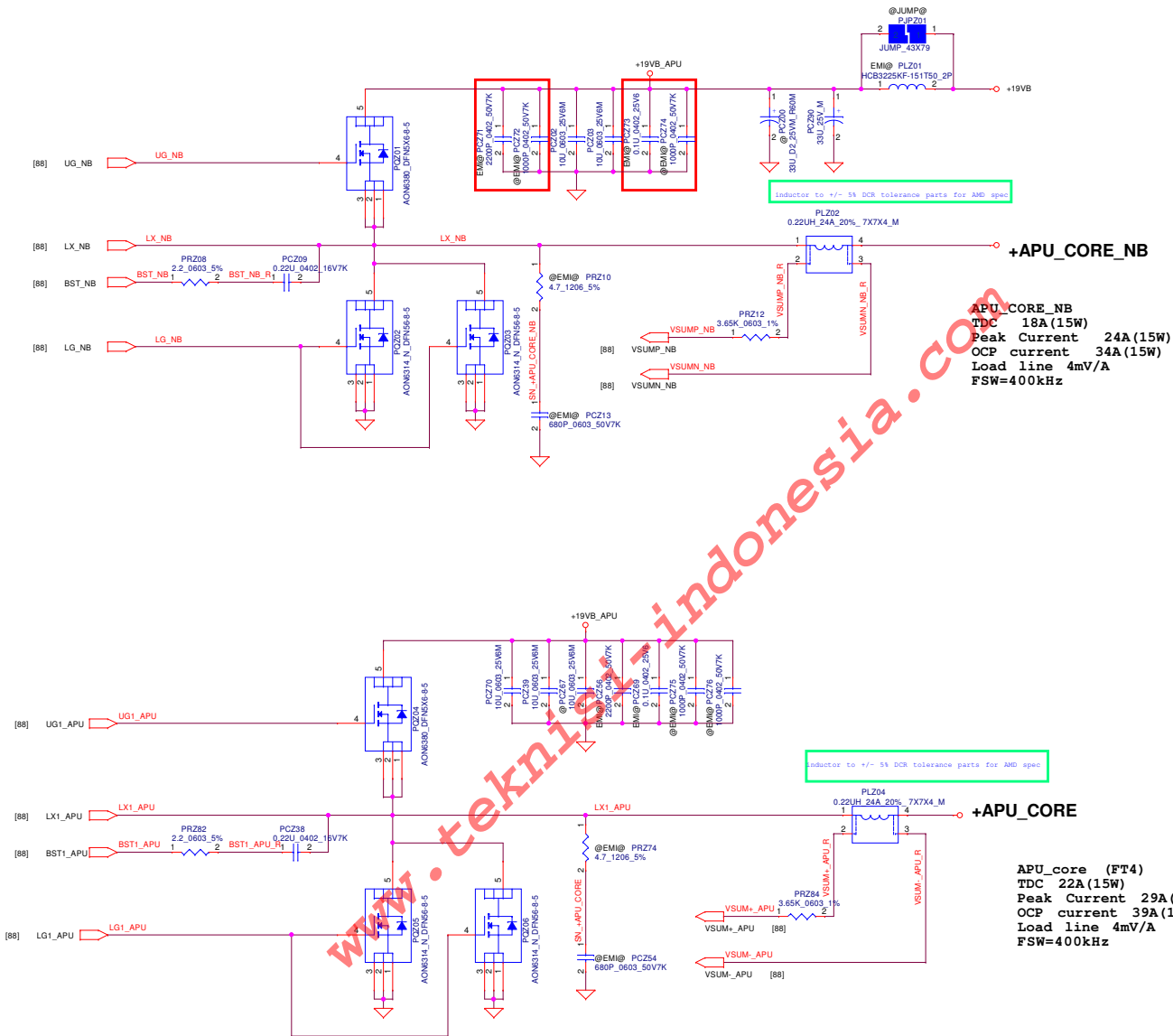
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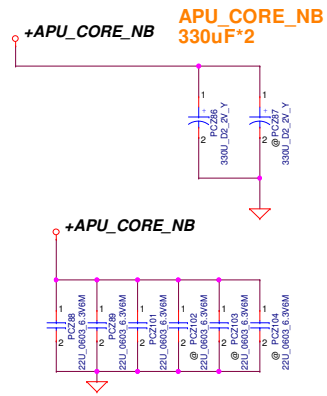
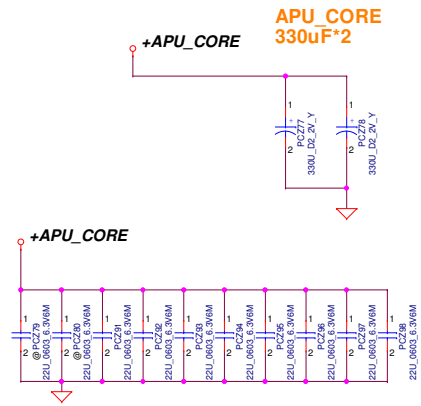


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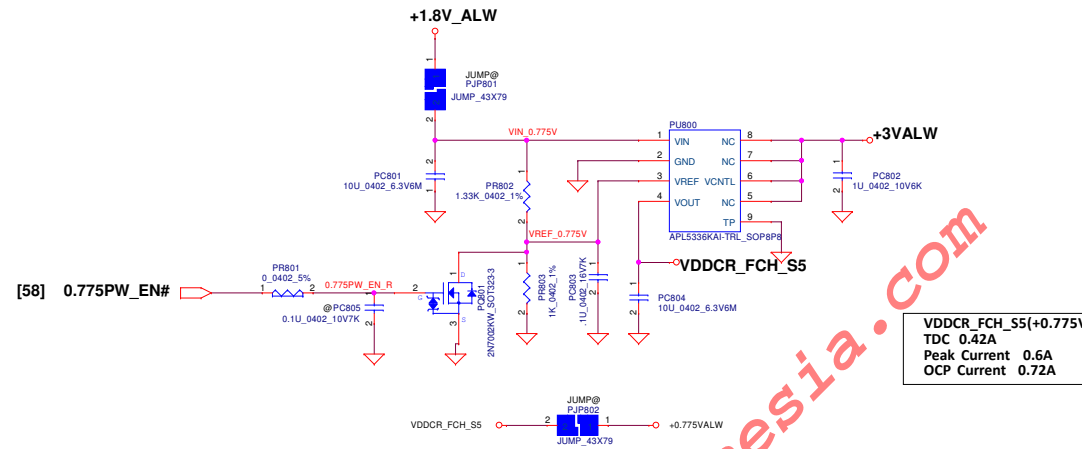


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The voltage level of 0.775PW_EN must be low




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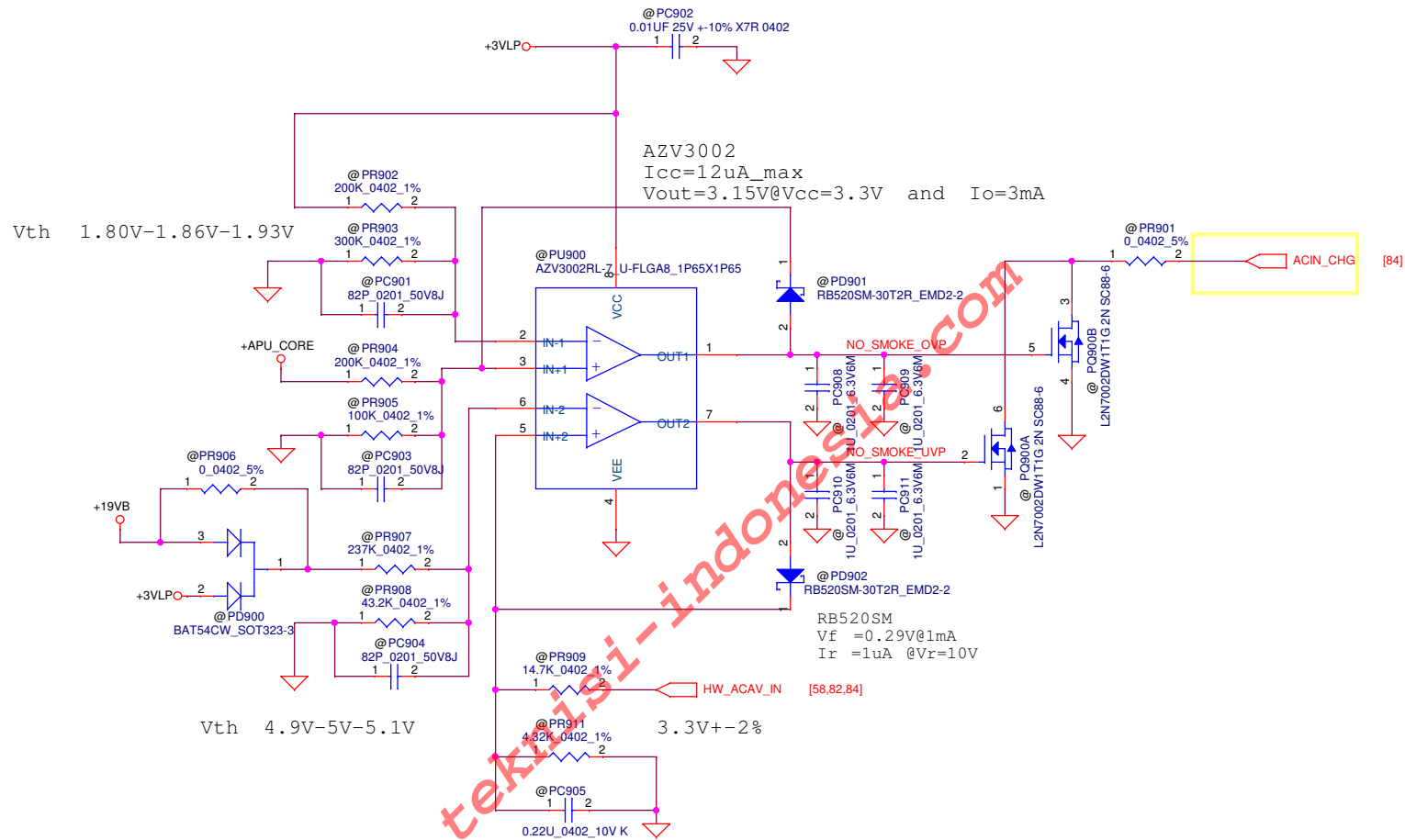
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